



SOI MAKES ELECTRONICS SIMPLY GREENER

Companies Collaborate to Exploit Semiconductor Technology
Enabling 30% to 40% Power Reduction for Chips and Systems

BOSTON, MASS., July 22, 2009 – The [SOI Industry Consortium](#) today announced the launch of SOI Simply Greener, an initiative encouraging broader application of the energy saving benefits of silicon-on-insulator (SOI) technology by the electronics industry. Semiconductor chips manufactured on SOI instead of traditional bulk silicon can realize energy savings of 30% or more when designed with the same feature size at equivalent performance. Broader adoption and usage of SOI technology by the electronics industry are consistent with global initiatives to both lower global electric power demand and reduce electric power bills for businesses and consumers.

“SOI is simply greener – and this story needs to be told,” said Horacio Mendez, Executive Director of the SOI Industry Consortium. “The first high-volume SOI applications were geared to high performance, but even there, the power-saving benefits are now apparent. The fact that 18 of the top 20 most power-efficient supercomputers [source: www.green500.org] are built with SOI demonstrates SOI’s ‘GreenIT’ benefits for enterprise applications. Also current versions of the top 3 consumer game consoles each include SOI-based chips, but much more can be done to help consumers lower their power bills through broader SOI usage. The SOI Consortium’s ‘green’ campaign will drive that point home to the design community.”

The energy-efficiency advantage of SOI technology contributes to both increased performance and reduced power consumption – the magnitude of benefit applied to each is the designer’s choice. Since “apples-to-apples” comparisons are impractical for most design teams to make, results from two studies are offered by consortium members to demonstrate this point.

- A benchmark analysis was performed by ARM Holdings using a 24-stage interconnect-loaded datapath circuit. When comparing IBM’s 45nm bulk silicon high performance and 45nm SOI technologies, the SOI implementation resulted in a 25% circuit area reduction, 66% reduction in static power leakage and nearly 22% reduction in dynamic power with 5% higher performance.
- A consumer product chip design that was migrated from 65nm bulk silicon high performance to IBM’s 45nm SOI technology realized a 50% increase in operating frequency, more than 64% reduction in die area and a 38% reduction in power consumption.

Whether designers put the emphasis on increasing or maintaining performance, significant power savings (as well as area savings) were realized with a move to SOI.

“As we detailed in our recent report [Semiconductor Technologies: The Potential to Revolutionize U.S. Energy Productivity](#), semiconductors already are the leading factor behind energy efficiency gains,” said lead author of the report John A. “Skip” Laitner, Director, Economic and Social Analysis, American Council for an Energy-Efficient Economy ([ACEEE](#)). “SOI offers a major advance in the power efficiency of electronics, and with appropriate public policy, investment and usage these semiconductor technology gains can

contribute to cumulative net electricity bill savings of \$800 billion through 2030 for consumers and businesses in the United States alone, as well as creating an average of 500,000 new jobs per year and reducing energy-related CO₂ emissions by more than 400 million metric tons annually over the period 2010 through 2030.”

In a [survey](#) jointly conducted last year by the [Global Semiconductor Alliance](#) and the SOI Industry Consortium, semiconductor designers indicated overwhelmingly that power savings is their primary driver for considering an SOI-based solution. To meet this market demand the 28 member companies, research and academic institutions of the SOI Industry Consortium are stepping up collaboration in the areas of new process development, chip design techniques, designer training, electronic design automation (EDA) productivity tools, and intellectual property (IP) development to provide broader access to SOI technology and ecosystem support for designers, and to enable the electronics industry, its customers and the global community to fully realize the power-saving advantages of this greener technology.

The SOI Industry Consortium welcomes companies, organizations, government and academic institutions to join the group in applying the full benefits of SOI-based electronics to global sustainability challenges and lowering the total cost-of-ownership of electronics. To find out more, to join or to arrange for a company-specific design clinic, please visit www.soiconsortium.org.

About the SOI Industry Consortium:

The SOI Industry Consortium is chartered with accelerating silicon-on-insulator (SOI) innovation into broad markets by promoting the benefits of SOI technology and reducing the barriers to adoption. Representing innovation leaders from the entire electronics industry infrastructure, current SOI Industry Consortium members include: AMD, Applied Materials, ARM, Cadence Design Systems, CEA-Léti, Chartered Semiconductor Manufacturing, Freescale Semiconductor, GLOBALFOUNDRIES, IBM, IMEC, Infotech, Innovative Silicon, KLA-Tencor, Magma Design, Nvidia, Ritsumeikan University, Samsung, Semico, SEH Europe, Soitec, Stanford University, STMicroelectronics, Synopsys, TSMC, Tyndall Institute, University of California-Berkeley, University Catholique de Louvain, and UMC. Membership is open to all companies and institutions throughout the electronics industry. For more information, please visit www.soiconsortium.org.

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