



THE SOI INDUSTRY CONSORTIUM ANNOUNCES RESULTS OF A SOI AND BULK FINFETS COMPARISON STUDY

SOI's Simpler Process Reduces Variability

BOSTON, MASS., October 21, 2009 – The [SOI Industry Consortium](#) today announced the results of a silicon-on-insulator (SOI) and bulk FinFETs comparison study conducted by the organization with the support of some of its key members. The study has evaluated performance, process variability, and cost differences between FinFETs fabricated with junction isolation on bulk silicon wafers, and FinFETs fabricated on SOI wafers. The analysis shows that fabrication on bulk and SOI wafers is for all practical purposes equivalent in performance and cost. However, bulk-based FinFETs are much more challenging to manufacture due to increased process variability.

Transistors are the miniscule on/off switches that make up the integrated circuits in today's microprocessors. The Fin Field Effect Transistor (FinFET) design relies upon a thin vertical silicon "fin" to help control leakage of current through the transistor when it is in the "off" stage. This design combination allows for the creation of new chips with enhanced performance and ever-shrinking geometries.

“This is a very important study. As the industry contemplates transitioning to non-planar transistors, it is vital to bring the best technical assessments possible of manufacturability, cost and performance between the two substrate options: bulk and SOI,” comments Horacio Mendez, executive director of the SOI Industry Consortium. “This collaborative effort between companies and R&D institutes takes a careful look at these critical parameters and its impact to end products.”

As the semiconductor industry looks toward the 22nm technology node, some manufacturers are considering a transition from traditional planar CMOS transistors to the three-dimensional FinFET device architecture. Relative to planar transistors, FinFETs offer improved channel control and therefore reduced short channel effects.

SOI simplifies FinFET fabrication: the buried oxide layer acts as an etch-stop and isolates individual transistors; the fin height is a function of the substrate thickness. Process variability comparisons showed that fin height and width are far more easily controlled in the SOI process.

In this study, the fin heights and widths of the FinFET pairs fabricated on bulk were shown to vary between 150 and 160% more than the SOI equivalents. Such variation in these “transistor matching characteristics”, which is the result of complexity in the bulk manufacturing process, can lead to significant end-product variability.

The SOI Industry Consortium welcomes companies, organizations, government and academic institutions to join the group in applying the full benefits of SOI-based electronics to global sustainability challenges and lowering the total cost-of-ownership of electronics.

About the SOI Industry Consortium:

The SOI Industry Consortium is chartered with accelerating silicon-on-insulator (SOI) innovation into broad markets by promoting the benefits of SOI technology and reducing the barriers to adoption. Representing innovation leaders from the entire electronics industry infrastructure, current SOI Industry Consortium members include: AMD, Applied Materials, ARM, Cadence Design Systems, CEA-Léti, Chartered Semiconductor Manufacturing, Freescale Semiconductor, GLOBALFOUNDRIES, IBM, IMEC, Infotech, Innovative Silicon, Kanazawa Institute of Technology , KLA-Tencor, Magma Design, Nvidia, Ritsumeikan University, Samsung, Semico, SEH Europe, Soitec, Stanford University, STMicroelectronics, Synopsys, TSMC, Tyndall Institute, University of California-Berkeley, University Catholique de Louvain, UMC and Varian. Membership is open to all companies and institutions throughout the electronics industry. For more information, please visit www.soiconsortium.org.

Press Contacts:

Camille Darnaud-Dufour
+33 (0) 6 79 49 51 43
camille.darnaud-dufour@soiconsortium.org

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