Smart power technology needs smart substrate

A. Rigny – Soitec, Business Development Manager
B. Aspar – Soitec, Business Unit General Manager
Soitec product portfolio adapted to wide markets

<table>
<thead>
<tr>
<th>Markets</th>
<th>Computing / Infrastructure</th>
<th>Consumer / Mobility</th>
<th>Automotive and industrial</th>
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<tbody>
<tr>
<td><strong>Applications</strong></td>
<td>Digital</td>
<td>Power / analog</td>
<td>RF</td>
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<td>Image sensors</td>
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<td>Photonics</td>
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<td>MEMS</td>
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<tr>
<td>Soitec products</td>
<td>FD-2D Premium SOI</td>
<td>Smart Power SOI</td>
<td>Wave SOI HRSOI-eSI</td>
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<td>FD-3D</td>
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<td>RF SOS</td>
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<td>Imager SOI Stacking for</td>
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<td>Imager</td>
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<td>Stacking for MEMS</td>
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</tbody>
</table>
Soitec – Leader in Engineered Substrates

Soitec Smart Power SOI™

Soitec Imager SOI™

Soitec RFSOI

SOI Smart Cut™ + EPI Layer

SOI Smart Cut™
Outline

1. Power market overview
2. BCDMOS and isolation technologies
3. Smart Cut™ SOI: a cost competitive technology
4. Conclusion
Wide range of application & Large market size

**Industrial**
- $2.5B/15.8%
  - Power grid
  - Medical
  - Home building

**Automotive**
- $5.6B/3.5%
  - Car, truck
  - EV/HEV

**Communication**
- $13.7B/7.6%
  - Smart phones, tablets

**Consumer**
- $3.1B/8%
  - Lighting
  - White goods

**IT**
- $4.6B/4.2%
  - Desktops
  - Fax, printers, scanners
  - Servers, NAS

*Market size $B / CAGR % (Source: IHS iSupply 2013)*
Smart power evolution

**Logic function (CMOS)**
Smart control
Interface to digital

**Basic power function (DMOS)**
Power conversion

**NVM Memory**
Store state
Smart evolution

**Control sensor**
Voltage/current overload
Temperature

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Integration examples

**LED lighting**
*Driver*
- Converting wall power for LED
- Dimming capability
- Remote control (wifi, bluetooth,...)

**Communication**
*AMOLED power supply*
- Positive and negative output supply
- Adjustable controlled output
- Thermal overload protection

**Automotive**
*Gate driver IC*
- Gate drivers for fast switches, high efficiency
- IC closer to engine
- Remote controlled

**Home building**
*Power over Ethernet*
- Delivery power through ethernet cable
- Large variety of point of load: flexible & configurable DC/DC converter

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BCDMOS platform for smart power

BiPolar + CMOS + DMOS = integration of Analog + logic + power functions
SMART POWER technology
Integration of different voltages

Key process is isolation

**PN junction isolation**
- Deep implant
- Large guard ring
- Surface penalty

**Deep trench isolation and PN junction**
- Deep trench for lateral isolation
- PN junction for vertical isolation
- Reduced surface penalty

**Deep trench isolation and SOI**
- Full isolation (lateral and vertical)
- Surface saving
- EMI immunity
Bulk low voltage and high voltage integration:

Electric isolation through pn-junctions

To isolate low voltage and high voltage areas:
Lateral pn-junction
Vertical pn-junction (impose a p substrate with n-epi layer)
Deep trench isolation:
*Electric isolation through dielectric trenches and pn-junctions*

**Low voltage (LDMOS)***
- Source
- Gate
- Drain
- n-doped epi layer
- P-well
- p+ junction isolation

**High voltage (LIGBT)***
- Source
- Gate
- Drain
- n+ n+ Drift region
- P-well
- p+ junction isolation

**Parasitic pn junction**

*Increase trench isolation breakdown through voltage divider concept*  
**Vertical pn-junction (impose a p substrate with n-epi layer)**
Dielectric isolation benefits:

*Silicon island enables different voltage integration*

Low voltage (LDMOS)

- Source
- Gate
- Drain

High voltage (LIGBT)

- Source
- Gate
- Drain

Isolation area

- Parasitic pn junction

Remove parasitic pn-junction

Improves leakage performances, thermal range operation

Source
Gate
Drain

n⁺

p⁺
P- well

n⁺

Drift region

p⁺
P- well

n⁺

n⁺

p⁺

p⁺

p- doped substrate

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SOI benefit at the device level

**SOI benefit at the device level**

*Improvement benefit by categories*

<table>
<thead>
<tr>
<th>Category</th>
<th>Benefit</th>
</tr>
</thead>
<tbody>
<tr>
<td>High temperature</td>
<td>Up to 225°C</td>
</tr>
<tr>
<td>No pn junction for p well</td>
<td></td>
</tr>
<tr>
<td>No pn junction with substrate</td>
<td></td>
</tr>
<tr>
<td>High reliability</td>
<td>True free latch-up</td>
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<tr>
<td>Low leakage</td>
<td></td>
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<tr>
<td>Low Rdson</td>
<td></td>
</tr>
<tr>
<td>High switching frequency</td>
<td></td>
</tr>
<tr>
<td>Performances</td>
<td>Rdson &lt; 1Ω cm (*)</td>
</tr>
<tr>
<td>Integration</td>
<td>Die shrink ~40%</td>
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<tr>
<td>Small trench isolation</td>
<td></td>
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<tr>
<td>Easy voltage stacking</td>
<td></td>
</tr>
<tr>
<td>Integration</td>
<td>Die shrink ~40%</td>
</tr>
<tr>
<td>Electrical isolation with substrate</td>
<td></td>
</tr>
<tr>
<td>Up to 600V IGBT integration</td>
<td></td>
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<tr>
<td>High voltage</td>
<td></td>
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</tbody>
</table>

*Piet Wessels, Migas 2009*
Die shrink enables cost effective solution
RESURF (Reduces Surface Field) Technology

How to guarantee a high Breakdown voltage

Fig. 2. Schematic equipotential lines and E-field in bulk and at the surface for various $t_{epi}$: (a) for 50µm at $BV=370$-$470V$; (b) for 15µm at $BV=1150V$ [after 2,2A].

Relationship between silicon thickness and doping concentration: to guarantee

electrical field in the drift region $\leq$ critical field (limit)
RESURF Technology in SOI

Two options

Option
thin SOI

SOI <0.5µm
Uniformity <0.05µm

Option
thick SOI

SOI >3µm
Uniformity <0.5µm

S. HU & Al, Int. Conf. on Communication, Circuits and Systems, ICCCAS 2008
SOI-BCDMOS flavors: Get more benefit from SOI

THICK SOI
Bulk like design

- Drain
- Gate
- Source

- Buried oxide layer
- Handle substrate

Dielectric isolation
- 1. Source, drain parasitic junction
- 2. Channel parasitic junction

- Channel parasitic junction

THIN SOI
Partially depleted

- Drain
- Gate
- Source

- Buried oxide layer
- Handle substrate

Dielectric isolation
- No source, drain parasitic junction

THIN SOI
Fully depleted

- Drain
- Gate
- Source

- Buried oxide layer
- Handle substrate

Dielectric isolation
- No source, drain parasitic junction
- No channel parasitic junction
SOI wafer technologies for power

**BSOI**
- Initial wafer
- Oxidation
- Bonding
- Grinding
- Finishing

SOI wafer

- Min SOI thickness ~ 3 µm
- Max SOI thickness ~ 100s µm
- Uniformity ~ 0.5 µm
- 2 wafers to build 1 SOI

**Smart Cut™**
- Initial wafer
- Oxidation
- Implantation
- Cleaning & bonding
- Splitting
- Finishing

SOI wafer

- Min SOI thickness ~ 0.1 µm
- Uniformity ~ 0.01 µm
- Max SOI thickness ~ few µm
- <2 wafers to build 1 SOI

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### Benefit at chip level and system level

**Thin SOI**
- Optimum RESURF
- High switching speed
- Lower Rdson
- No latch-up
- Very smaller devices
- Trench isolation

**Thick SOI**
- Non optimal RESURF
- Switching speed
- Small Rdson
- No latch-up
- Small devices
- Deep trench isolation

**Bulk**
- Non optimal resurf
- Switching speed
- Small Rdson
- Latch-up
- Large devices
- Junction isolation

**SYSTEM**
- System size/weight
- Total BOM cost
- ESD/EMI protection
- Medium current

**SYSTEM**
- System size/weight
- Total BOM cost
- ESD/EMI protection
- High current

**SYSTEM**
- System size/weight
- Total BOM cost
- ESD/EMI protection
- High current
SOI penetration in power market

Industrial
- Ultrasound Medical imaging
- Oil drilling
- Aerospace

Automotive
- Transceiver CAN/LIN
- Brushless motor drive
- High T. gate drivers

Communication
- AMOLED power supply
- AC/DC Power converter

Consumer
- LED drivers
- 3-phase motor drivers (white good, air conditioner)
- Plasma display drivers

IT
- Desktop power supply
- Power over Ethernet

CAGR_{2013-2016} power market = 7%
CAGR_{2013-2016} power SOI smart cut™ = 20%

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Conclusion

1. **Power market is going smart**
   - Power distribution is going Smart grid
   - Remote control of all power consumption for better global efficiency

2. **Mix-voltage integration is key**
   - Integrate different voltage requirements for remote control, logic, sensor, power conversion
   - Enable power efficiency (conversion and usage)

3. **SOI provides better performances and smaller die**
   - Simplify design cycle for time to market
   - High temperature and truly latch-up free operation
   - Thin SOI-BCDMOS design brings additional benefits (switching speed, low $R_{dson}$)

4. **SOI for smart power is cost effective**
   - Substrate performance impacts on chip design, size and cost
   - Optimized SOI design per application enable high competitive solution
Thank you for your attention