Our Business
We are worldwide leaders in the design, manufacture and supply of semiconductors, electronic components and solutions.
We are Innovators in Electronics.

Our Strengths
• Advanced RF, mixed signal and materials technology
• Broad and vertically integrated product portfolio
• Extensive global manufacturing and sales network

Our Figures
• Net sales 14 billion USD*
• Employees 77,751*
• Number of locations 102* (30 in Japan, 72 overseas)
• Established in 1944

*as of March 31, 2019
Vision to Reality – CMOS Won

Conventional RF Front End

CMOS Transceiver

Our Vision

UltraCMOS® Integrated RF Front End

Timeline of Key Innovations

2000

2020

Antenna Switches

MMMB Switches

RFFE Tuning

Tunable Filters

Low Noise Amplifiers

Power Amplifiers

mmWave RFFE

In Production

Sampling
Combining the Best of the Best

Most Widely Used Semiconductor Technology

CMOS
- Scalable
- Lowest Power and Cost
- Fabless Model

Highly Insulating Substrate

SAPPHIRE + HR SILICON
- Proven SOI Technology
- Outstanding RF Properties
- RF + Digital + Analog + Passive Integration

Industry-leading RF Semiconductor Technology

Combining the Best of the Best
- Unique Position in Industry
- Better Performance
- Highly Scalable
- Enables Integration
- Proven Global Fabless Model
• Reduced bulk parasitics
• Fully-depleted is preferred for no kink effect
• Faster devices
• Reduced $CV^2f$ power loss
• Improved linearity
• High isolation
• High passive Q

Sapphire Substrate Eliminates Bulk Nonlinear Capacitances
What Does RF SOI Enable?

- FET stacking allows UltraCMOS® technology to handle high RF power levels (> +40 dBm)
  - Higher power handling will NOT degrade performance
  - Stacking creates a virtual high-voltage CMOS FET that can handle high power levels
- High power handling requires low-loss, insulating substrate
  - Bulk-CMOS will not work due to conducting substrate
SOI Accumulation Capacitance and Charge

• Bulk CMOS accumulates in deep subthreshold because of hole source from P+ well contact
• SOS will accumulate from EHP generation (thermal/light/etc.)
• Charged is trapped in channel by reverse-biased PN junctions
  – Forms anti-series diodes
• Creates harmonics with RF excitation
  – Charge sloshing

Simulated charge accumulation with RF signal present
HaRP™ Invention: Linearity Breakthrough

IM3 vs Relative Phase between Duplexer and Switch
PTX = +20 dBm, PBL = -15 dBm

-80
-85
-90
-95
-100
-105
-110
-115
-120

0 50 100 150 200

Relative phase @ f = 1.76GHz

SP6T

SP6T + HaRP™ Technology

> 25 dBm

IM3 Specification

3GPP Intermodulation Specification

GSM Cell

WCDMA Phone

Interference

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25 September 2019
HaRP™ Technology Impact

Cellular Switch Market Share

2005
Before HaRP™

Today & Tomorrow

SOI  GaAs
UltraCMOS® Technology Evolution

- 300 mm: Gross Die per 12" Wafer
  - >25,000
  - 60% smaller
  - 20x better linearity

- 200 mm: Gross Die per 8" Wafer
  - >85,000
  - 50% smaller
  - 10x better linearity

- 150 mm: Gross Die per 6" Wafer
  - 9,000
  - 25% smaller
  - 4x better linearity

- 60 nm
- 130 nm
- 0.35 μm
UltraCMOS® Technology IP: Value to the Industry

IEEE SPECTRUM Patent Power Scorecard 2017

Company by Pipeline Power

- Intel Corp.: 4,000
- Taiwan Semiconductor Manufacturing Co.: 3,454
- Cirrus Logic Inc.: 2,998
- Samsung Electronics Co.: 2,608
- Semiconductor Energy Laboratory Co.: 1,671
- InvenSense Corp. (Xperi Corp.): 1,255
- Cavium Inc.: 1,247
- Sandisk LLC (Western Digital Corp.): 1,183
- GlobalFoundries Inc.: 997
- pSemi (a Murata Company): 967
- Skyworks Solutions Inc.: 927
- Texas Instruments Inc.: 843
- Everspin Technologies Inc.: 780
- Marvell Technology Group Ltd.: 644
- Rambus Inc.: 627
- InvenSense Inc.: 588
- Infineon Technologies AG: 584
- Avago Technologies Ltd.: 545
- Xperi Corp. (formerly Tessera Holdings): 532
- Sunpower Corp. (Total SA): 506

TOP 10 Semiconductor Manufacturing
THE FUTURE: Appears We Were Right

- Monolithic multichannel FULLY Integrated RF Front End
  - 28 GHz and 39 GHz

RFFE = SOI
Our Foreseeable Future

8-Channel mmW RFFE – Sampling
THANK YOU