# GAP9 IoT Application Processor

## Intelligence at the very edge of the network

GAP9 is an IoT application processor that enables massive deployment of low-cost, battery operated intelligent devices that capture, analyse, classify and act on multiple streams of rich data such as images, sounds, radar or vibrations.

GAP9 is uniquely optimized to execute a large spectrum of image and audio algorithms including convolution neural network inference with extreme energy efficiency.

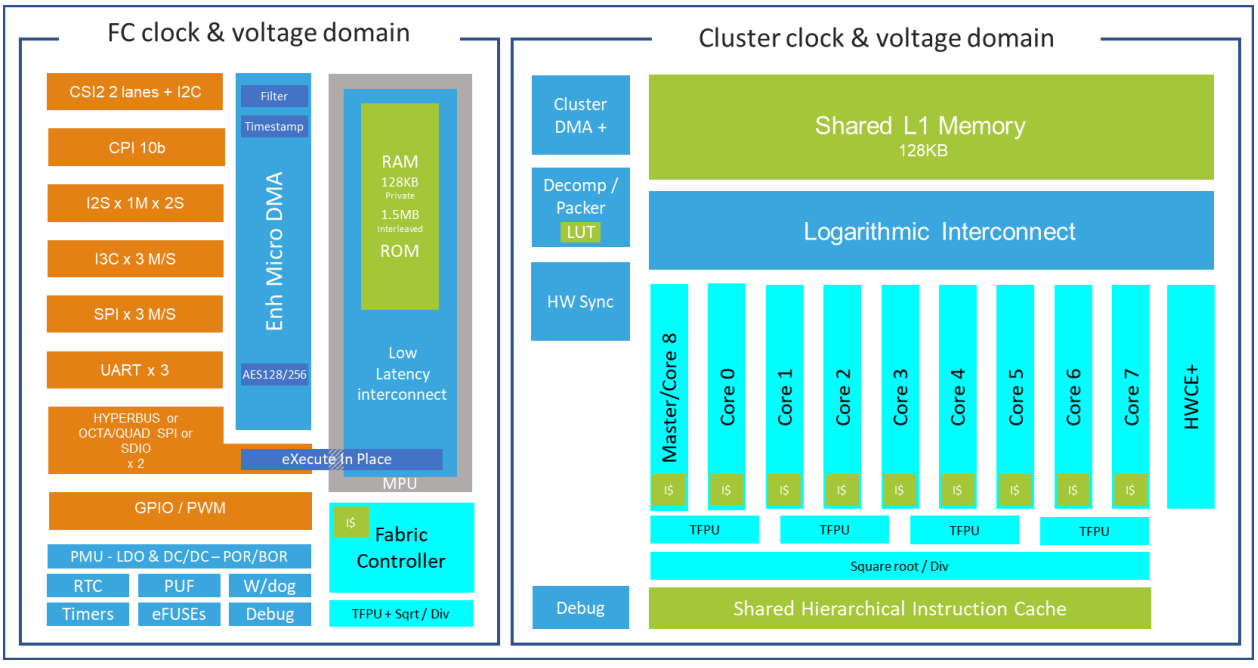
GAP9 allows industrial and consumer product manufacturers to integrate artificial intelligence, advanced classification and signal processing into new classes of battery operated wireless edge devices for IoT applications including next generation intelligent wearables, people and object classification, home security, sound classification, consumer robotics and smart toys.

By enabling autonomous operation GAP9 dramatically reduces deployment and operating costs of a wide range of intelligent edge devices.

## Highlights

- **Enable Artificial Intelligence and signal processing in highly power constrained devices**
- **Allow devices to react to information in fusions of images, sounds and vibrations**
- **Reduce network traffic and power consumption by interpreting data on device**
- **Eliminate data privacy concerns through local analysis**
- **Highly integrated design brings low total system cost**

## Hierarchical Processor Architecture




**GAP9 Block Diagram**

GAP9's hierarchical, demand-driven architecture enables ultra-low-power operation by combining:

- A series of highly autonomous smart I/O peripherals for connection to cameras, microphones and other capture and control devices
- A high bandwidth, low-power internal and external memory system with virtual memory support
- A fabric controller (FC) core for control, communications and security functions
- A compute cluster of 9 cores incorporating a Convolutional Neural Network accelerator (HWCE)
- Highly efficient, explicit memory management hardware and software

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## Applications

GAP9 can be used in a wide range of applications where there is a need to process and interpret rich data on highly power constrained devices such as:

| | |
|---|---|
| People demographics | Security systems |
| Road monitoring | Activity detection |
| Consumer robotics | Autonomous navigation |
| Wearables / Hearables | Audio / video signal processing |
| Vital sign monitoring | Sound classification |
| Geophysics sensing | Surveillance camera |
| Inattention detection | Machine health monitoring |

## Developing on GAP9

**GAP9 hardware development kits will be available for purchase in the first half of 2020. Please contact GreenWaves Technologies directly for more details**

## GAP9 Features

### Performance

- Core performance of 10µW/MHz
- Up to 250 MHz (FC) 400 MHz (Cluster) internal clock
- Cluster executes 28 GOPS at a few tens of mWs
- FC executes 2 GOPS at a few mWs
- HWCE executes 5x5 convolution 16 bit-fixed point in one cycle. - 20 GOPS on convolutions at a few mWs
- 1µA deep sleep current
- 1µA to retain each of the four 32kB banks of L2 non-interleaved memory
- 0.8V down to 0.5V core VDD supply
- 1.8V for I/Os
- 0.4ms cold boot time
- 2µs to power and start cluster
- 1mW low power awake state with wake-up time of a few microseconds

### Architecture Efficiency

- 10 identical high performance, extended ISA, RISC-V ISA cores
- Dynamic voltage & frequency scaling and automatic body biasing
- Multiple power states: deep sleep, deep sleep with retentive RAM, low activity, SOC on, SOC on & cluster on
- Fabric controller (FC) core for control and communication
- Cluster of 9 cores for compute-intensive tasks:
  - Logarithmic interconnect
  - Hardware event synchronization
  - Hierarchical, shared instruction cache
  - Hardware Convolution Engine (HWCE) for Convolution Neural Networks
- Software controlled explicit data movement across the memory hierarchy
  - Multi-channel 1D/2D cluster DMA with integrated data decompressor / packer / unpacker.
  - Specialized multi-channel micro-DMA for autonomous peripheral support (hardware filtering, timestamping)

### Hardware Features

- Fabric controller core: 1KB instruction cache
- Cluster:
  - 128KB shared data memory
  - 16KB hierarchical, shared instruction cache
- All cores support RV32 I, M, C, & F ISA and custom ISA extensions for DSP, Bit Manipulation and Vector/SIMD operations.
- Transprecision floating-point support for IEEE 32-bit and 16-bit and alternate 16-bit and 8-bit float formats
- Hardware support for 16, 8, 4 and 2-bit fixed point and 16 and 8-bit floating point vectors
- µDMA streamed data filtering and timestamping
- On-the-fly hardware AES128/256 encryption / decryption
- Programmable Voltage Regulator
- Real-time clock
- 2 programmable clocks
- Secured execution support with Memory Protection Unit
- 1.5MB interleaved + 128KB non-interleaved retentive L2 Memory
- Optional external high-speed low power SDRAM and Flash with mappable virtual memory support
- Execute in place (XIP) support
- 32 kHz external quartz
- BGA 7mmx7mm and WL-CSP 3.5mm x 3.5mm package options

### I/O Interfaces

- MIPI CSI-2 - 2 lanes
- 10-bit Camera Parallel Interface (CPI)
- 3 x SPI Master/Slave
- 3 x I3C Master/Slave
- 3 x I2S (1 master/slave & 2 slave) Multi channel TDM support
- 3 x U(S)ART with hardware flow control
- 2 x switchable HyperBus, Quad-SPI, Octo-SPI, SDIO DDR/SDR memory interfaces
- GPIO / PWM
- JTAG

### Tools

- RISC-V C / C++ toolchain with added optimizations based on GNU toolset (GCC & GDB)
- GAP AutoTiler code generator for explicit memory movement
- GAP*Flow* toolset providing end-to-end code generation from NN frameworks
- PULP OS, FreeRTOS™, Zephyr OS, AliOS Things & Arm® Mbed™ OS support
- Cross OS PMSIS cluster & device API
- Debug support including on-chip debug
- GVSOC SoC Simulator with wave generation
- PlatformIO based cross-platform IDE and debugger

### Libraries

- Parallelized, vectorized and highly optimized software components:
- Data Analysis (FFT, MFCC, etc.)
- Deep Learning (CNN/DNN based)
- Image Processing (HOG, DOG, Viola-Jones, etc.)

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