Ultra High Efficiency
Mixed Signal Processors

Shenzhen & Zurich
Problems in front of AI

1. How to continuously improve computing efficiency, subjecting to Moore's law?
2. How to get more effective data?
3. How to reduce computing costs?
4. How to achieve on-chip learning, not just inference?

Top1 vs. operations, size \( \propto \) parameters

Intel CPU Trends

- Moore's Law
- Dennard Scaling
- Effective end of Moore’s law, and much of the claimed gain in density is offset by the fact that much of the new circuits must be devoted to error correction
- Dennard Scaling Ends

(sources: Intel, Wikipedia, K. Okutani)
**REEXEN Technology, devoted to mixed signal computing**

### Chip Design Team

<table>
<thead>
<tr>
<th>Qualifications</th>
<th>Average Industry experience of over 10 years, with a number of mass production experience</th>
</tr>
</thead>
<tbody>
<tr>
<td>Background</td>
<td>Huawei, IMEC, Xilinx, ARM, Qualcomm, ETH, Nanyang Technological University</td>
</tr>
<tr>
<td>Papers</td>
<td>ISSCC, JSSCC, TCAS, Frontiers in Neuromorphic, Engineering, etc</td>
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### Algorithm Team

<table>
<thead>
<tr>
<th>Qualifications</th>
<th>Industry experience of nearly 10 years</th>
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<tbody>
<tr>
<td>Background</td>
<td>Tencent, Chinese academy of sciences, Imperial College London, Munich university of technology</td>
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80% R&D

40% hold doctor degree

Company Profile

**Zurich Office**
- Founded in Dec 2017

**Shenzhen Office**
- Founded in Jun 2018
Human brain has an average of $10^{11}$ neurons and can carry out complex processing and learning with power consumption of only: 20 W

One game of AlphaGo costs thousands of dollars in electricity. Power efficiency of most digital AI chips: 1-5 tops /W
Biological neurons

Analog computation, digital propagation, computation & storage are both done in neurons

Most AI chips

Storage and Computation Separated
IBM Research AI Hardware Center is developing a roadmap for 1,000x improvement in AI compute performance efficiency over the next decade, with a pipeline of Digital AI Cores and Analog AI Cores.

**Technology Features**

- **Unique mixed signal computing chip IP (Deep Neural Network)**
  - Deep Neural Network
- **Very High energy efficiency**
  - 20-50Tops/W
  - Ultra-high energy efficiency
  - 10 times higher than current digital accelerators
- **Low cost**
  - On chip storage, saving power consumption on DDR driver and DRAM
- **Adjustable accuracy**
  - Programmable bit precision

**Technology**

![Diagram showing technology features with a focus on energy efficiency and performance](image-url)
More than 90% are focusing on digital NN accelerators

### AI Chip Landscape

<table>
<thead>
<tr>
<th>Tech Giants/Systems</th>
<th>IC Vendor/Fabless</th>
<th>IP/Design Service</th>
<th>Startup in China</th>
<th>Startup Worldwide</th>
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<tbody>
<tr>
<td>Google</td>
<td>Intel</td>
<td>arm</td>
<td>Cambicon</td>
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<td>SYNOPSYS</td>
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<td>Renesas</td>
<td>Hail</td>
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<td>SiFive</td>
<td>Hail</td>
<td>Tachyten</td>
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<tr>
<td>Intel</td>
<td>Qualcomm</td>
<td>Firefly</td>
<td>Hail</td>
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Reexen chip architecture

ADA: Analog- Digital Acceleration

To Ada Lovelace, the world's first computer programmer
Analog and analog-digital computers were there

Such analog computers were used, among other things, for NASA's Mercury, Gemini, and Apollo programs.

Photo: NASA

Analog computer used 1912-1965.

Photo: Steven Fine
Advantages of analog computation

- More efficient and less costly for most basic mathematical computation because signal is continuous
- Easier to realize the integration of data acquisition and data processing as sensory information is analog
- More effective to realize complex mathematical computation related to on chip learning
Comparison of mixed signal computing vs. digital computing: multiplier and adder

E.g.

- **8 bit multiplier:**
  - Analog: 4-10
  - Digital: 3000+

- **8 bit adder:**
  - Analog: one wire
  - Digital: 200+
Analog vs digital circuits: power consumption and area requirements to get the same SNR

Source: Hosticka, “Performance comparison of analog and digital circuits”
Difficulties of analog/mixed signal circuits design

Difficult to design

Noise, nonlinearity and mismatch
Latency-vs-accuracy tradeoff of float vs. integer-only MobileNets on ImageNet using Snapdragon 821 big core.

Deep neural network: More tolerant for noise and low bit precision; At 8bit integer precision, nearly no accuracy drop comparing to float precision.

Source: Google Inc 2018 CVPR, “Quantization and Training of Neural Networks for Efficient Integer-Arithmetic-Only Inference”
Appendix-Review of state-of-art NN accelerator

Phase domain, time domain, voltage domain or current domain

**Phase domain:** Kentaro Yoshioka VLSI 2018

**Time domain:** Anvesha Amravat ISSCC 2019

**Conclusion:**
- Noise is determined the fundamental physics law for all analog circuit with whatever domain.
- Every doubling the power, the SNR is improved by 3 dB.

![Diagram](image_url)

**Mixed-signal**

Scale with process

Hard

Easy


[B. Murmann, Asilomar 2015]
FD-SOI provides choice between speed and power

**Ultra-Thin BODY**
Excellent Electrostatic Control of the channel
Low SCE, DIBL $\rightarrow$ Low $V_t$ @ High $V_D$
Gate length shrink $\rightarrow$ continue device scaling

**Undoped Channel & no Pocket**
Less $V_t$ variability & SRAM $V_{min}$ improved
Lower Power Consumption
Reduce Temperature dependency & no RDF

**Total Dielectric Isolation**
Lower SD capacitances & Lower SD Leakage
Less Sensitive to Temperature
Higher power efficiency
Source: Coventor Blog

**Ultra Thin BOX**
Body Biasing (BB) $\rightarrow$ FBB & RBB
Speed boost due to BB
GP Implantation $\rightarrow$ $V_t$ adjustment
FD-SOI provides higher potential for System on Chip Integration

<table>
<thead>
<tr>
<th>Mobility</th>
<th>IoT</th>
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| **Best Power/Perf/Cost solution for**
Low-mid tier Baseband + AP
4G transceiver integration | **Perfect fit for wireless & ULP/U LL IoT clients in need of:**
On-demand processing performance
Integrated RF
Embedded memory
Cost effective |

<table>
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<th>5G &amp; Radars</th>
<th>Automotive</th>
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| **Ideal technology for**
single chip solution with integrated PA <6GHz applications (transceivers) w/ 35-50% die shrink (vs 28 poly) for LTE, Wifi and other wireless applications | **Unique advantages in low power/ high reliability**
ADAS (<5W) for autonomous driving |

Source: Soitec
High Speed Vision Processing Chip Series Based on ADA Architecture

Efficient vision processing chip ADA100V

### Applications
- AI-assisted education
- Driving assistance
- Augmented/virtual Reality
- Home security & monitoring

### Features
- Ultra high computing Efficiency: 25~50Tops/W
- Mixed signal computing in memory
- Reduced latency and support high - speed image/video processing
- Reduced chip ad system temperature, improve reliability
- Support AI processing by battery power

Scene application
Vision processing chip application scenarios

- Reducing latency to support high-speed image and video processing
- Reduce the temperature of chips and systems to improve reliability
- Intelligent Processing for Battery Power Supply

**Global AI chip segment size**

- Video monitoring: 0.33 (2017) → 1.82 (2022E)
- Autopilot: 0.85 (2017) → 5.2 (2022E)

**Data source:** CICC

**Global smart home devices shipments**


**Data source:** IDC

Scene application
<table>
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<th>Features</th>
<th></th>
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<td>Sub-micro watt voice activity detection for smart wake-up of devices</td>
<td></td>
</tr>
<tr>
<td>Key word spotting and speaker identification for smart control of</td>
<td>wearable devices and home/car appliances.</td>
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Chip features:

- High efficiency
- Low cost
- Reduced latency & bandwidth
- Privacy Protection
- High integration
- Flexibility & on-chip learning

Technical Advantage
Connect intelligent devices "True" wirelessly

Remove the wire for not only data transfer but also for power
Contact us

Wechat

Website

Twitter

Reexen Technology

Shenzhen & Zurich